IN THE SPECIFICATION:

Page 1, paragraph beginning at line 21, is amended as follows:

--A conventional method for manufacturing a MOS transistor will be described with reference to FIGS. 1a through ~~1d~~ 1c.--

Page 1, paragraph beginning at line 23, is amended as follows:

Referring first to FIG. 1a, ~~polysilicon for use as a gate oxide layer 3 and a gate electrode 4 is~~ oxide layer 3 as a gate oxide and polysilicon for use as a gate electrode 4 are formed at a predetermined width on a surface of a device region of a silicon wafer 1. The device region of the silicon wafer 1 is defined by a field oxide layer 2, which is formed by a LOCOS (local oxidation of silicon) process or a trench process. Next, using the gate electrode 4 as a mask, ion injection using a p-type or n-type dopant at a low concentration is performed on the device region of the silicon wafer 1. As a result, LDDs (lightly doped drains) 5 are formed on the device region of the silicon wafer 1, and side walls 6 are formed to both sides of the gate oxide layer 3 and the gate electrode 4.

Page 6, paragraph beginning at line 13, is amended as follows:

Subsequently, using a sputtering process, titanium is deposited to a thickness of approximately ~~300~500~~ 300~500Å over the entire surface of the silicon wafer 21, then rapid thermal processing (RTP) is performed for 20~40 seconds and at a temperature of approximately 700~800°C while flowing nitrogen at a flow rate of 50sccm.

Page 6, paragraph beginning at line 17, is amended as follows:

A titanium silicide layer 28 is formed by the reaction between the titanium and silicon. That is, the silicon of the gate electrode 24 and the source/drain 27 reacts with the titanium to form the titanium silicide 28. Since the silicon does not react with the titanium of the side walls 26 and the ~~filed~~ field oxide layer 22, the titanium on these elements is left remaining as non-reacted titanium. The non-reacted titanium is removed using a solvent so that it does not interfere with device operation.

Page 7, paragraph beginning at line 18, is amended as follows:

Subsequently, with reference to FIG. 2d, a BPSG layer 30 is deposited to a thickness of approximately ~~10,000 20,000Å~~ 10,000~20,000Å using SACVD. SACVD is performed at a temperature of approximately 500°C and a pressure of approximately 200 Torr. To increase the strength of the BPSG layer 30, heat treating is performed at a temperature of 600~800°C and for 30~50 seconds to realize densification.

Page 8, paragraph beginning at line 12, is amended as follows:

Further, since the BPSG layer 30 may be formed in the same SACVD deposition chamber that the ozone process is performed in, that is, since the BPSG layer 30 may be formed without interruption following the ozone process, contact with the air outside the chamber is prevented. This isolation of the silicon wafer 21 from the air, which is a supply source for ~~nitrogen~~ hydrogen, prevents the situation where boron ions are generated as a result of the presence of ~~nitrogen~~ hydrogen. Ultimately, the leakage of current resulting from the diffusion of boron ions into the silicon wafer 21 does not occur, and the resulting ~~heating~~ degradation of the transistor is prevented.